IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Randolph

Serial No.: 10/032,646

Conf. No.: 5662

Filed: December 27, 2001

Title: PLANAR TRANSISTOR STRUCTURE USING ISOLATION IMPLANTS FOR IMPROVED VSS RESISTANCE AND FOR PROCESS SIMPLIFICATION

Art Group: 2811

Examiner: Loke, Steven Ho Yin

Mail Stop AF
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

In response to the Office Action mailed September 29, 2003 (Paper No. 7), with a three-month shortened statutory period for response set to expire on December 29, 2003, please amend the Application as follows:

CERTIFICATION UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 16, 2003.

Toni Stanley
Signature

Toni Stanley
(Printed name of person certifying)